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(11) EP 1 291 629 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:  
12.03.2003 Bulletin 2003/11

(51) Int Cl.7: G01J 5/34

(21) Application number: 02005045.6

(22) Date of filing: 06.03.2002

(84) Designated Contracting States:  
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE TR  
Designated Extension States:  
AL LT LV MK RO SI

- Ikari, Motoo  
Kadoma-shi, Osaka 571-8686 (JP)
- Takada, Yuji  
Kadoma-shi, Osaka 571-8686 (JP)
- Matsuda, Hiroshi  
Kadoma-shi, Osaka 571-8686 (JP)
- Murayama, Yorinobu  
Kadoma-shi, Osaka 571-8686 (JP)

(30) Priority: 10.09.2001 JP 2001273653

(71) Applicant: Matsushita Electric Works, Ltd.  
Kadoma-shi, Osaka-fu 571-8686 (JP)

(74) Representative: Appelt, Christian W.  
Boehmert & Boehmert  
Pettenkoferstrasse 20-22  
80336 München (DE)

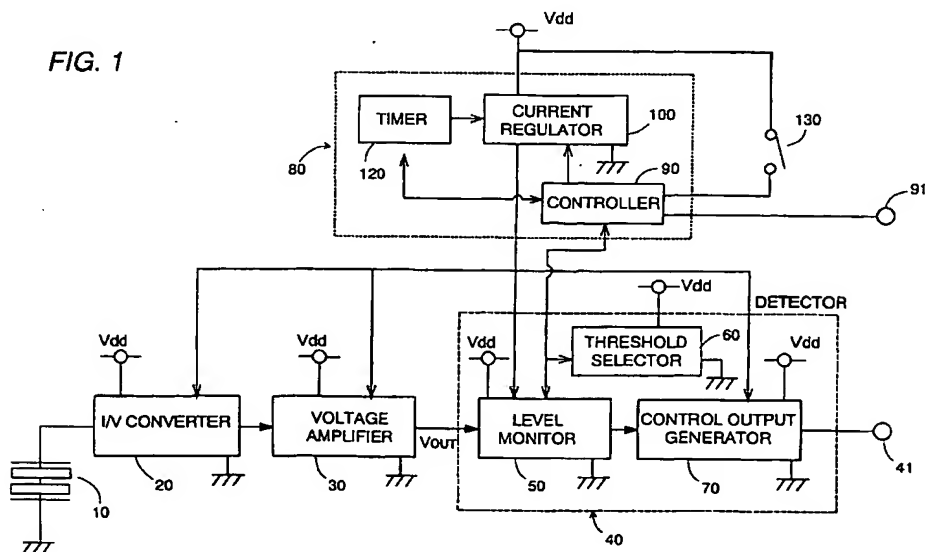
(72) Inventors:  
• Hironaka, Atsushi  
Kadoma-shi, Osaka 571-8686 (JP)

(54) Object detecting device with a pyroelectric sensor

(57) An object detecting device utilizes a pyroelectric sensor providing a sensing current, a voltage amplifier providing an amplified voltage proportional to the sensing current, and a level monitor providing a detection signal when the amplified voltage exceeds a detection threshold. The device has a standby mode where the voltage amplifier receives a limited source current to provide the voltage of low amplification, and the level

monitor provides a wake-up signal when the low amplified voltage exceeds a preliminary threshold lower than the detection threshold. In response to the wake-up signal, the device is switched to an operation mode where the amplifier receives a rated source current to provide a voltage of high amplification for comparison with the detection threshold. Thus, the amplifier is kept to be less-power consuming in the absence of the wake-up signal, reducing a power requirement.

FIG. 1



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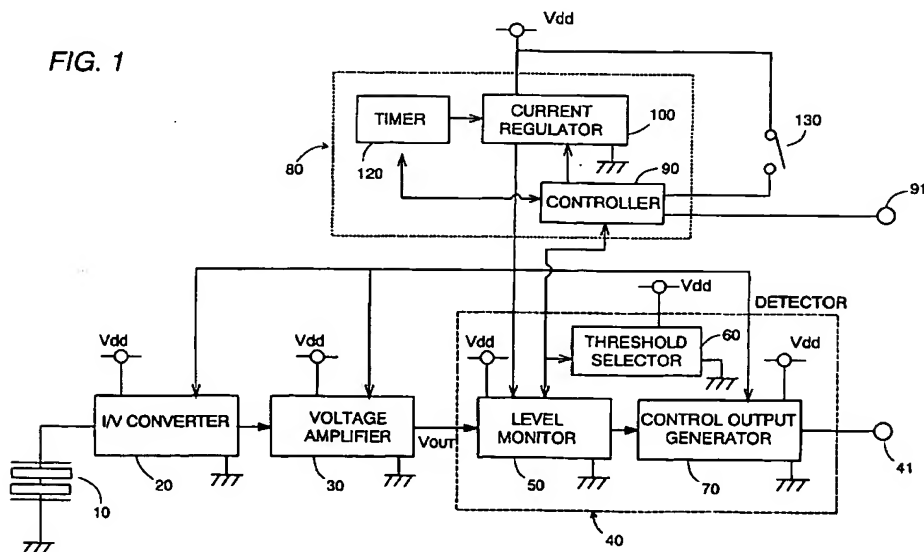
(74) Representative: **Appelt, Christian W.**  
**Boehmert & Boehmert**  
**Pettenkoferstrasse 20-22**  
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**(54) Object detecting device with a pyroelectric sensor**

(57) An object detecting device utilizes a pyroelectric sensor providing a sensing current, a voltage amplifier providing an amplified voltage proportional to the sensing current, and a level monitor providing a detection signal when the amplified voltage exceeds a detection threshold. The device has a standby mode where the voltage amplifier receives a limited source current to provide the voltage of low amplification, and the level

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FIG. 1



make a dedicated function such as turning on an illumination appliance in response to the control output, thereby reducing the power consumption.

[0006] In order to start the device rapidly for reliable detection, the mode selector is preferred to supply an initialization current greater than the rated source current to the voltage amplifier only for a predetermined initialization time period immediately upon energization of the device. Further, the mode selector is preferred to select the rest mode for a predetermined stabilization time period immediately subsequent to the initialization time period, and to switch the rest mode into the standby mode thereafter. Thus, the voltage amplifier inherently requiring much initialization current can be rapidly made ready for reliable operation. After the stabilization time period, the components of the device can be made stable to be ready for reliable detection, while eliminating a possibility of causing erroneous circuit operation leading to a false detection due to unstable outputs of the voltage amplifier during the stabilization time period.

[0007] The voltage amplifier may be of two-stage amplifier having a front-stage amplifying section and a rear-stage amplifying section. In this connection, the mode selector is configured to supply the limited source current to the front-stage and rear-stage amplifying sections in the standby mode, and supply the limited source current to the front-stage amplifying section and the rated source current to the rear-stage amplifying section in the operation mode. With the use of the two-stage amplifier and the associated scheme of only changing the level of the current being fed to the rear-stage amplifying section, it is made possible to further reduce the power consumption as compared to a case where the entire current to the amplifier is changed from the limited level to the rated level.

[0008] Further, the voltage amplifier is preferred to generate the rated voltage output which saturates at a level just above the detection threshold for the purpose of minimizing the power consumption in the operation mode, yet retaining reliable detection.

[0009] Preferably, the threshold selector includes a first voltage divider providing the preliminary threshold from a reference voltage and a second voltage divider providing the detection threshold from the same reference voltage. The first voltage divider is composed of a series combination of first resistors, while the second voltage divider is composed of a series combination of second resistors. The first resistor is selected to have a higher resistance than the second resistor in order to realize an advantageous effect of reducing the power consumption made at the first voltage divider to give the preliminary threshold with the use of the first resistors of high resistance, while enabling the second voltage divider to give the detection threshold accurately with the use of the second resistors of low resistance. Because of that first and second resistors are preferably selected from those that can be integrated in a chip for circuit miniaturization of the device, and also because

of that the resistors of the type available can give an accurate resistance value as the intended resistance lowers, the second voltage divider makes the use of the second resistors of low resistance to provide the accurate the detection threshold for reliable object detection therewith, while the first voltage divider can consume less power with the use of the first resistors of high resistance in providing the preliminary threshold which is not critical for object determination and could be rough as compared to the detection threshold. For instance, the first resistor may be selected from a non impurity-doped polysilicon resistor and a MOS (metal oxide semiconductor) transistor, while the second resistor may be selected from an impurity-doped polysilicon resistor.

[0010] These and still other objects and advantageous features of the present invention will become more apparent from the following description of a preferred embodiment when taken in conjunction with the attached drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

### [0011]

FIG 1 is a block diagram showing a circuit of an object detecting device in accordance with a preferred embodiment of the present invention;

FIG. 2 is a circuit diagram showing a current regulator and its associated circuits of the above device;

FIG. 3 is a circuit diagram of a voltage amplifier utilized in the above device;

FIG. 4 is a waveform chart illustrating the operation of the above device;

FIG. 5 is a waveform chart illustrating an operation of the mode selector;

FIG. 6 is a circuit diagram of a threshold selector utilized in the above device;

FIG. 7 is a circuit diagram showing a modified current regulator and its associated circuit applicable to the above device; and

FIG. 8 is a circuit diagram of a voltage amplifier utilized in connection with the above modified current regulator.

## MODE FOR CARRYING OUT THE INVENTION

[0012] Referring now to FIG. 1, there is shown an object detecting device in accordance with a preferred embodiment of the present invention. The device is utilized for surveillance of a room or the like space and is adapted to be interlocked with an external device such as an illumination appliance, an alarm and the like for activating the external device upon detection of a human body in the room. The device utilizes a pyroelectric sensor which generates a sensing current in proportion to changes in the amount of incident infrared radiation from the human body. The sensing current is fed to an I/V converter where it is converted into a corresponding

voltage. The voltage is then amplified at a voltage amplifier 30 to provide a voltage output to a detector 40 for detection of the human body. The amplifier 30 has an offset voltage  $V_{OFF}$  around which the voltage output  $V_{OUT}$  varies, as shown in FIG. 4, in proportion to the amount of the sensing current from the pyroelectric sensor 10.

[0013] The detector 40 includes a level monitor 50, a threshold selector 60 providing two thresholds, namely, a preliminary threshold  $TH_1$  and a detection threshold  $TH_2 (>TH_1)$  to the level monitor 50, and a control output generator 70. The voltage output  $V_{OUT}$  from the amplifier 30 is compared at the level monitor 50 selectively with  $TH_1$  ( $-TH_1$ ) and  $TH_2$  ( $-TH_2$ ) to generate a wake-up signal when the voltage output satisfies a relation that  $V_{OUT} > TH_1$  or  $V_{OUT} < -TH_1$ , and to generate a detection signal when the voltage output satisfies a relation that  $V_{OUT} > TH_2$  or  $V_{OUT} < -TH_2$ . The control output generator 70 is provided to issue, in response to the detection signal, a control output at an output terminal 41 for activating the external device. As will be discussed later, the wake-up signal is utilized to switch a standby mode, which is a default mode of consuming less power, to an operation mode for reliable detection of the object. The standby mode is defined to provide a limited source current to the I/V converter 20, the voltage amplifier 30, the level monitor 50, and the control output generator 70 for activating the same at a minimum performance level, while the operation mode is defined to provide a rated source current higher than the limited current to the same for activating the same at its full capability to obtain a reliable and consistent detection result.

[0014] For this purpose, the device is provided with a mode selector 80 which includes a controller 90, a current regulator 100, and a timer 120. The controller 90 is provided to switch the standby mode to the operation mode and vice versa. The current regulator 100 is configured to flow source currents of different levels designated by the controller 90. The source currents include the limited source current of about  $0.03 \mu A$  to  $0.09 \mu A$ , for example, the rated source current of about  $0.18 \mu A$  to  $0.6 \mu A$ , for example, and an initialization current higher than the rated current. As shown in FIG. 2, the current regulator 100 includes a constant current supply 101, a plurality of FETs 102 to 107, and switches 111 to 113. The constant current supply 101 supplies a reference current  $I_{101}$  from a power source  $V_{dd}$  through FET 102, while a series combination of FETs 103 and 104 is connected across the series combination of the current supply 101 and FET 102 to flow a mirror current  $I_{103}$ . Connected across FET 104 are three sets of series combinations each composed of each one of switches 111 to 113 and each one of FETs 105 to 107, as illustrated, such that the mirror current  $I_{103}$  can vary by selective closing and opening of switches 111 to 113. As the mirror current  $I_{103}$  varies, the I/V converter 20, the voltage amplifier 30, the level monitor 50, and control output generator 70 that are connected to receive a corre-

spondingly varied voltage will be supplied with one of the limited source current, the rated source current, and the initialization source current. For instance, as illustrated in the figure, the voltage amplifier 30 includes two FETs 33 and 34 of which gates are connected to receive the voltage corresponding to the mirror current  $I_{103}$  in order to flow currents  $I_{33}$  and  $I_{34}$  as one of the limited source current, the rated source current, and the initialization source current from the power source  $V_{dd}$ . Whereby, the voltage amplifier 30 can be selectively made to provide the restricted voltage output proportional to the voltage from the I/V converter 20, to provide the rated voltage output proportional to the voltage from the I/V converter 20, and to complete the initialization, as will be discussed later.

[0015] As shown in FIG 3, the voltage amplifier 30 is of a two-stage amplifier including a front-stage amplifying section 31 and a rear-stage amplifying section 32. These sections 31 and 32 include current regulating FETs 33 and 34 which respond to the mirror current  $I_{103}$  flowing through the current regulator 100 for flowing the source currents  $I_{33}$  and  $I_{34}$  from the power source  $V_{dd}$  to the front-stage amplifying section 31 and the rear-stage amplifying section 32, respectively. The gates of FETs 31 and 32 are commonly connected to receive the voltage corresponding to the mirror current  $I_{103}$  at a current control input 35. The front-stage amplifying section 31 includes a reference voltage input 36 for receiving a predetermined reference voltage and a voltage input 37 for receiving the voltage from the I/V converter 20 to amplify the same. The rear-stage amplifying section 32 includes an output terminal 38 for providing the amplified output to the level monitor 50.

[0016] Also, the I/V converter 20 is of two-stage configuration having two parallel current regulating FETs 23 and 24 which are connected between the power source  $V_{dd}$  and the ground and of which gates are connected to receive the voltage corresponding to the current  $I_{103}$  in order to flow currents  $I_{23}$  and  $I_{24}$  as one of the limited source current, the rated source current, and the initialization source current, thereby providing the corresponding output to the voltage amplifier 30. Likewise, the level monitor 50 and the output controller 70 include current regulating FETs 53 and 73 respectively in order to flow individual currents  $I_{53}$  and  $I_{73}$  as one of the above different source currents. It is noted in this connection that these source currents  $I_{33}$ ,  $I_{34}$ ,  $I_{23}$ ,  $I_{24}$ ,  $I_{53}$  and  $I_{73}$  may be made different from each other by selecting the corresponding FETs of different characteristics.

[0017] The controller 90 is normally set to make the standby mode in which the current regulator 100 responds to flow the limited source currents, and the threshold selector 42 is normally set to give the preliminary threshold  $TH_1$  to the level monitor 50 so that the level monitor 50 takes the voltage output  $V_{OUT}$  as the restricted voltage from the voltage amplifier 30, i.e., the voltage of low amplification and compares it with the preliminary threshold  $TH_1$ . When it is found that  $V_{OUT} > TH_1$

or  $V_{OUT} < -TH_1$ , as shown in FIG. 4, the level monitor 50 provides the wake-up signal to the threshold selector 60 as well as to the controller 90 of the mode selector 80. Upon this occurrence, the threshold level selector 60 gives the detection threshold  $V_{TH2}$  to the level monitor 50, and at the same time the controller 90 selects the operation mode to cause the amplifier 30 to provide the voltage output  $V_{OUT}$  as the rated voltage output, i. e., the voltage of high amplification. Thus, the level monitor 50 is enabled to compare the voltage output  $V_{OUT}$  with the detection threshold  $TH_2$  and issue the detection signal when  $V_{OUT} > TH_1$  or  $V_{OUT} < -TH_1$ . The detection signal is indicative of the presence of the human body and is converted into the control signal for activating the external device.

[0018] When the detection signal is issued, the controller 90 responds to activate the timer 120 to start counting time and switches the operation mode back to the standby mode after the timer counting a predetermined time frame  $T$ , thereby making the device to be ready for checking the next wake-up signal. In addition, the controller 90 constantly checks whether or not subsequent detection signal is issued within the time frame  $T$ , and resets the timer 120 to start counting time each time the subsequent detection signal is acknowledged within the time frame  $T$ , thereby extending the time frame  $T$  so long as the detection signal appears successively for notifying such event to the external device.

[0019] The controller 90 is optionally provided with a reset terminal 91 for receiving a reset signal from the external device. When connecting the reset terminal 91 to the external device, the controller 90 is set to select a rest mode once the detection signal is acknowledged and keeps the rest mode until receiving a reset signal from the external device. The rest mode is defined to keep supplying the limited source current to the I/V converter 20, the amplifier 30, the level monitor 50, and the control output generator 70, and at the same time disabling the level monitor 50, i.e., neglecting the result of the level monitor 50. Thus, it is possible to minimize the power consumption while the external device is responding, yet avoiding the occurrence of the wake-up signal which would provoke the operation mode. This is particularly advantageous when the external device is only required to activate for a limited time interval in response to the first advent of the detection signal.

[0020] In order to reduce the power consumption at the amplifier 30 once the detection signal is issued, the amplifier 30 may be selected to saturate the voltage output  $V_{OUT}$  just above the detection threshold  $TH_2$  or just below  $-TH_2$  when supplied with the rated source current, as shown in FIG. 5.

[0021] As shown in FIG. 6, the threshold selector 60 includes a first voltage divider providing the preliminary threshold  $TH_1$  and a second voltage divider providing the detection threshold  $TH_2$  to the level monitor 50. The first voltage divider is a series combination of first resistors 61 connected in series with a switch 63 between

the power source  $V_{dd}$  and the ground, while the second voltage divider is a series combination of second resistors 62 connected in series with a switch 64 between the power source and the ground. The connection between the first resistors 61 is connected through a switch 65 to the level monitor 50, while the connection between the second resistors 62 is connected through a switch 66 to the level monitor. Normally, the switches 63 and 65 are closed to provide the preliminary threshold  $TH_1$  to the level monitor 50. When receiving the wake-up signal from the level monitor 50, the switches 64 and 66 are closed to provide the detection threshold  $TH_2$  to the level monitor 50. In view of that the preliminary threshold may be rough as it does not critical to the detection of the human body, while the detection threshold have to be accurate for reliable detection, and also that available resistors elements capable of being integrated in a semiconductor chip together with other electronic components of the device exhibit more accurate resistance value as the resistance value lowers, it is contemplated in the present invention to use the first resistors 61 having the higher resistance and the second resistors 62 of lower resistance. Whereby, it is possible to give the reliable human detection with the accurately determined detection threshold, yet reducing the power consumption in providing the preliminary threshold with the use of the first resistors of high resistance. For instance, the first resistor 61 is selected from a non impurity-doped polysilicon resistor or MOS (metal oxide semiconductor) transistor, while the second resistor 62 is selected from impurity-doped polysilicon resistor.

[0022] Further, the device is designed to become stable rapidly upon being energized for immediate and reliable object detection. For this purpose, the controller 90 responds to the throw-in of a power switch 130 of the device for providing an initialization time period during which the initialization current higher than the rated current is allowed to flow in the I/V converter 20 and the voltage amplifier 30 for rapidly making these high current-consuming circuits operative, and the limited current is allowed to flow to the level monitor 50 and the control output generator 60 of less current-consuming circuits. Immediately thereafter, the controller 90 selects the rest mode of disabling the output of the level monitor 50 for a predetermined stabilization time during which the limited source current is supplied to make the whole circuits stable to be ready for reliable detection free from any erroneous operation due to unstable outputs from the individual circuits, particularly from the I/V converter 20 and the voltage amplifier 30. Thereafter, the controller 90 switches the rest mode to the standby mode, enabling the output of the level monitor 50 for making the intended operation of detecting the human body.

[0023] FIGS. 7 and 8 show a modified current regulator 100A and associated circuits which are similar to those utilized in the above embodiment but are configured to switch the current being supplied to the rear-stage amplifier of the I/V converter 20 and the rear-stage

amplifier of the voltage amplifier 30, while constantly flowing the limited source current to the front-stage amplifiers of the I/V converter 20, the front-stage amplifier of the voltage amplifier 30, the level monitor 50, and the control output generator 70. In this connection, the amplifier 30 is configured, as shown in FIG. 8, so that FET 33 of the front-stage amplifying section 31 and FET 34 of the rear-stage amplifying section 32 have individual gates to receive currents  $I_{103A}$  and  $I_{103B}$  of different levels or different voltage from the current regulator 100A, respectively through current control inputs 35A and 35B. As shown in FIG. 7, the current regulator 100A includes, in addition to a series combination of a constant current supply 101A and FET 102A connected across the power source Vdd, a front-end current generator 121 composed of FETs 103A, 104A and 105A and a switch 111A to provide a front-end mirror current  $I_{103A}$ , and a rear-end current generator 122 composed of FETs 103B, 104B and 105B, and switches 111B, 112B and 113B to provide a rear-end mirror current  $I_{103B}$ . The front-end mirror current  $I_{103A}$  is applied as a corresponding voltage to the gate of current regulating FET 23 of the front-stage amplifying section 21 of the I/V converter 20, the gate of current regulating FET 33 of the front-stage amplifying section 31 of the amplifier 30, the gate of current regulating FET 53 of the level monitor 50, and the gate of the current regulating FET 73 of the control output generator 70 in order to flow the limited source currents  $I_{23}$ ,  $I_{33}$ ,  $I_{53}$ , and  $I_{73}$  from the power source Vdd to the individual circuits 20, 30, 50, and 70. Likewise, the rear-end mirror current  $I_{103B}$  is applied as a corresponding voltage to the gate of current regulating FET 24 of the rear-stage amplifying section 22 of the I/V converter 20, the gate of current regulating FET 34 of the rear-stage amplifying section 32 of the amplifier 30 in order to flow currents  $I_{24}$  and  $I_{34}$  from the power source Vdd to the rear-stage amplifying sections as one of the limited source current, rated source current, and the initialization current by selective activation of the switches 111B, 112B, and 113B.

[0024] In the absence of the wake-up signal from the level monitor 50, the controller 90 of the mode selector 80 sets the switches 111B, 112B, and 113B of the rear-end current generator 122 to make the rear-end mirror current  $I_{103B}$  nearly equal to the front-end mirror current  $I_{103A}$ , thereby flowing the limited source current  $I_{24}$  and  $I_{34}$ , which are nearly equal to those currents  $I_{23}$ ,  $I_{33}$ ,  $I_{53}$ ,  $I_{73}$  caused by the front-end mirror current  $I_{103A}$ , to the rear-stage amplifying sections of the I/V converter 20 and the amplifier 30. When the wake-up signal is acknowledged, the controller 90 is switched to provide the rear-end mirror current  $I_{103B}$  larger than the front-end mirror current  $I_{103A}$ , thereby flowing the rated source current  $I_{24}$  and  $I_{34}$ , which are greater than those currents  $I_{23}$ ,  $I_{33}$ ,  $I_{53}$ ,  $I_{73}$  caused by the front-end mirror current  $I_{103A}$ , to the rear-stage amplifying section of the I/V converter 20 and the amplifier 30. Thus, when the device is switched into the operation mode, the rated currents of

high level can be supplied only to the rear-stage amplifying sections of the I/V converter 20 and the amplifier 30 for the intended performance, thereby avoiding unnecessary high current consumption otherwise made at the front-stage amplifying sections. The high initialization current required at the very beginning of energizing the device can be fed only to the rear-stage amplifying sections of the I/V converter 20 and the amplifier 30 while the limited source currents are fed to the front-stage amplifying sections of the I/V converter 20 and the amplifier 30, as well as to the level monitor 50 and the control output generator 70. In this sense, the current regulator 100A is also configured to provide the initialization current higher than the rated source current by selective activation of switches 111B to 113B.

[0025] The features disclosed in the foregoing description, in the claims and/or in the accompanying drawings may, both separately and in any combination thereof, be material for realising the invention in diverse forms thereof.

#### Claims

1. An object detecting device comprising:

a pyroelectric sensor (10) generating a sensing current in accordance with changes in the amount of infrared radiation incident on said sensor from an object;  
an I/V converter (20) which converts said sensing current from said pyroelectric sensor into a corresponding voltage;  
a voltage amplifier (30) which amplifies said voltage from the I/V converter into an amplified voltage;  
a detector (40) including a level monitor (50) which compares said amplified voltage with a predetermined detection threshold ( $TH_2$ ) to provide a detection signal when said amplified voltage satisfies a detection criterion with regard to said threshold, said detector responding to said detection signal for issuing a control output which is indicative of the detection of the object and is adapted to actuate an external device;

#### characterized in that

said voltage amplifier provides a restricted voltage output of low amplitude when receiving a limited source current and provides a rated voltage output of high amplitude when receiving a rated source current greater than said limited source current,

said detector includes a threshold selector (60) which has said detection threshold ( $TH_2$ ) and a preliminary threshold ( $TH_1$ ) lower than said detection threshold, and which is normally set to provide

the preliminary threshold to said level monitor,

said level monitor compares said restricted voltage output from said voltage amplifier with the preliminary threshold to provide a wake-up signal when the restricted voltage output satisfies a preliminary criteria with regard to said preliminary threshold;

said threshold selector switches said preliminary threshold to said detection threshold in response to said wake-up signal; and

said device further includes a mode selector (80) which, in response to the wake-up signal, provides an operation mode for supplying said rated source current from a power source to said voltage amplifier such that said level monitor compares the rated voltage output with said detection threshold for detection of the object, and otherwise provides a standby mode for supplying said limited source current to said voltage amplifier from said power source.

2. The object detecting device as set forth in claim 1, wherein

said mode selector (80) keeps said operation mode continuously for a predetermined time frame from the first advent of the detection signal and switches back forcibly to the standby mode thereafter.

3. The object detecting device as set forth in claim 2, wherein

said mode selector (80) resets said time frame to start each time said detection signal is followed by another detection signal within said time frame.

4. The object detecting device as set forth in claim 1, wherein

said mode selector has a reset input (91) for receiving a reset signal from said external device, said mode selector switching said operation mode forcibly into a rest mode for keeping said limited source current to supply to said voltage amplifier from said power source and at the same time disabling said level monitor upon seeing the first advent of said detection, and keeping said rest mode until receiving said reset signal at said reset input.

5. The object detecting device as set forth in claim 1, wherein

said mode selector supplies an initializing current greater than said rated current to said voltage amplifier only for a predetermined initialization time period immediately upon energization of the device.

6. The object detecting device as set forth in claim 5, wherein

said mode selector selects a rest mode of

supplying said limited source current to said amplifier while disabling said level monitor for a predetermined stabilization time period immediately subsequent to said initialization time period, and switches the reset mode into said standby mode thereafter.

7. The object detecting device as set forth in claim 7, wherein

said voltage amplifier (30) is of two-stage amplifier having a front-stage amplifying section (31) and a rear-stage amplifying section (32),

said mode selector supplying said limited source current to said front-stage and rear-stage amplifying sections in said standby mode, and supplying said limited source current to said front-stage amplifying section and supplying said rated source current to said rear-stage amplifying section in said operation mode.

8. The object detecting device as set forth in claim 1, wherein

said voltage amplifier provides said rated voltage output which saturates at a level just above said detection threshold.

9. The object detecting device as set forth in claim 1, wherein

said mode selector supplies the limited source current to said I/V converter (20) in said standby mode, and supplies the rated source current to said I/V converter in said operation mode.

10. The object detecting device as set forth in claim 1, wherein

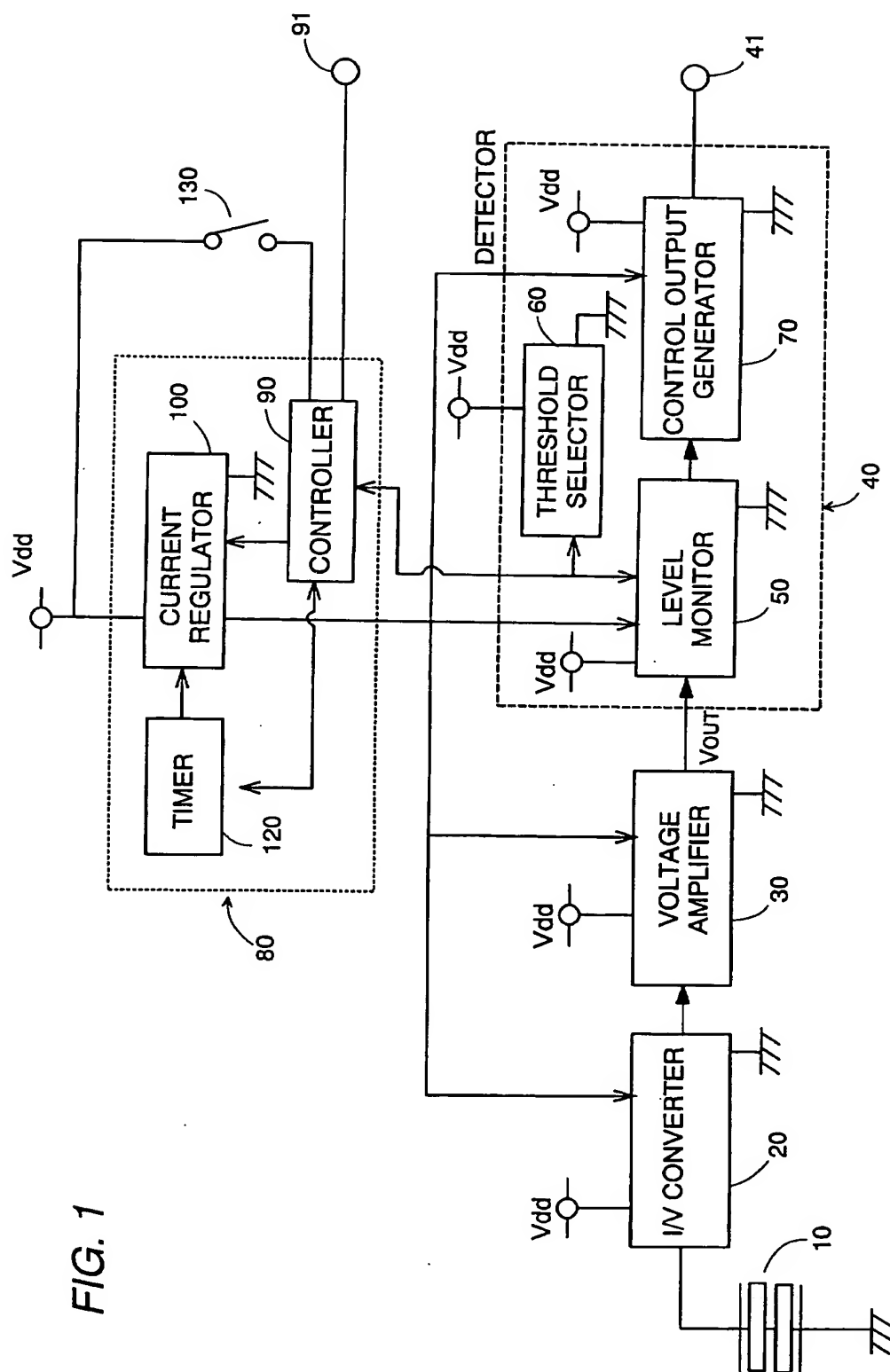
said threshold selector (60) comprises a first voltage divider composed of a series combination of first resistors (61) to provide said preliminary threshold ( $TH_1$ ) from a reference voltage, and a second voltage divider composed of a series combination of second resistors (62) to provide said detection threshold ( $TH_2$ ) from said reference voltage source, said first resistors having higher resistance than said second resistors.

11. The object detecting device as set forth in claim 10, wherein

said first resistor is selected from a non impurity-doped polysilicon resistor, while said second resistor is selected from an impurity-doped polysilicon resistor.

12. The object detecting device as set forth in claim 10, wherein

said first resistors is selected from a MOS transistor, while said second resistor is selected from an impurity doped polysilicon resistor.



**FIG. 1**



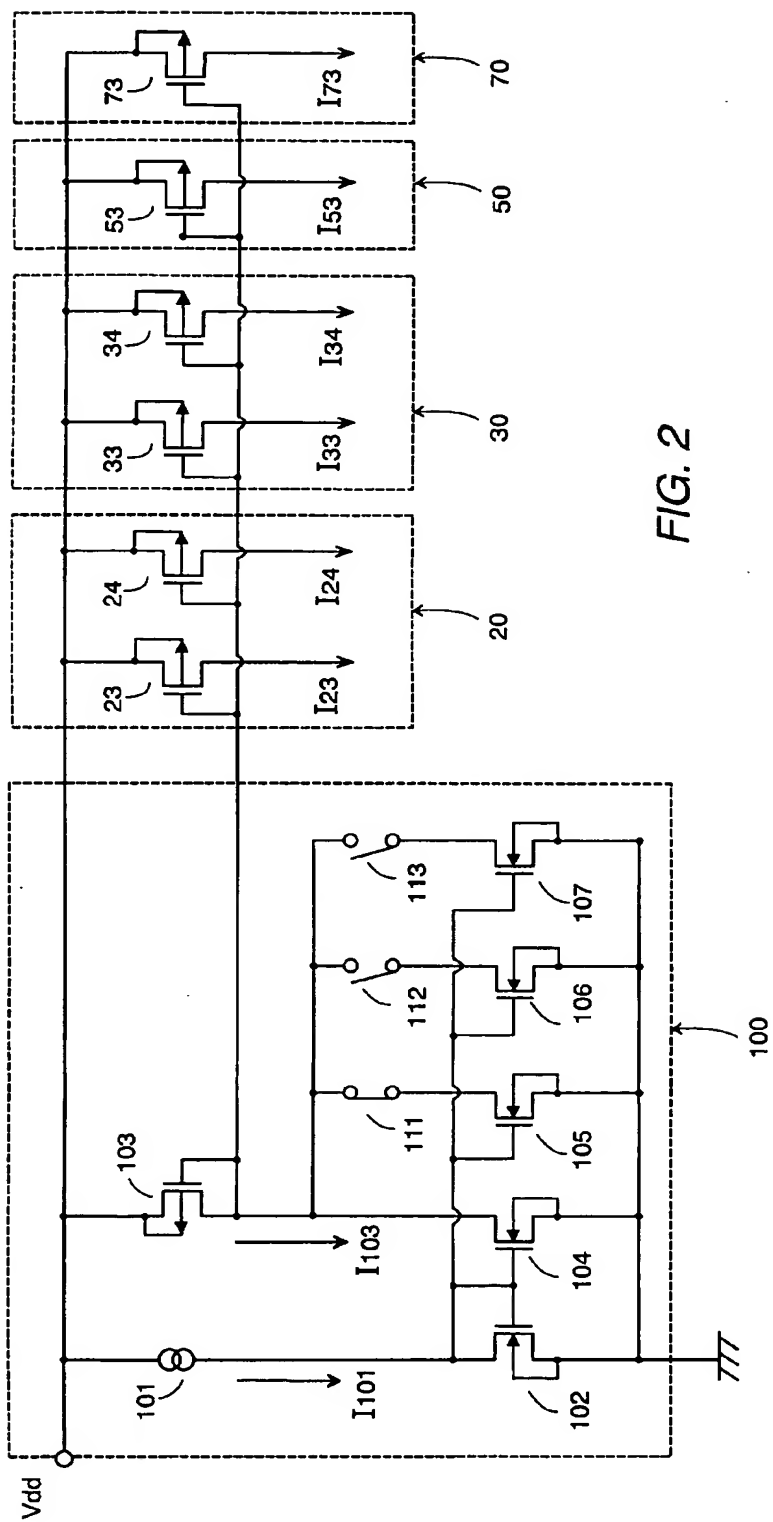
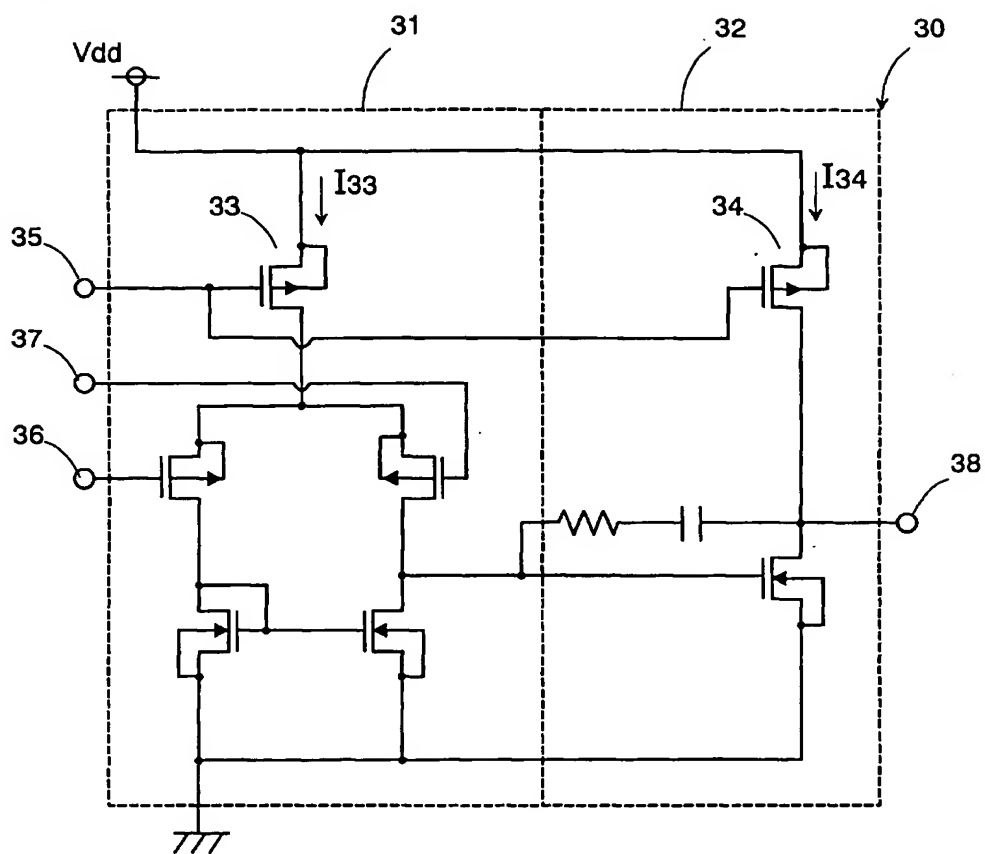


FIG. 2

FIG. 3



**FIG. 5**

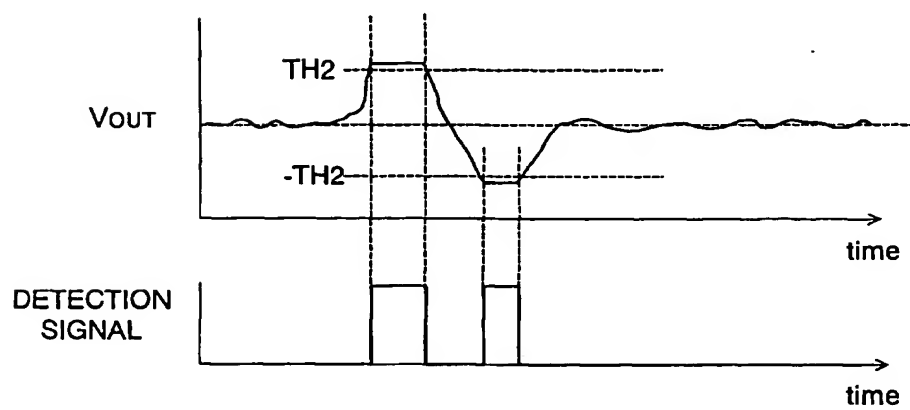


FIG. 4

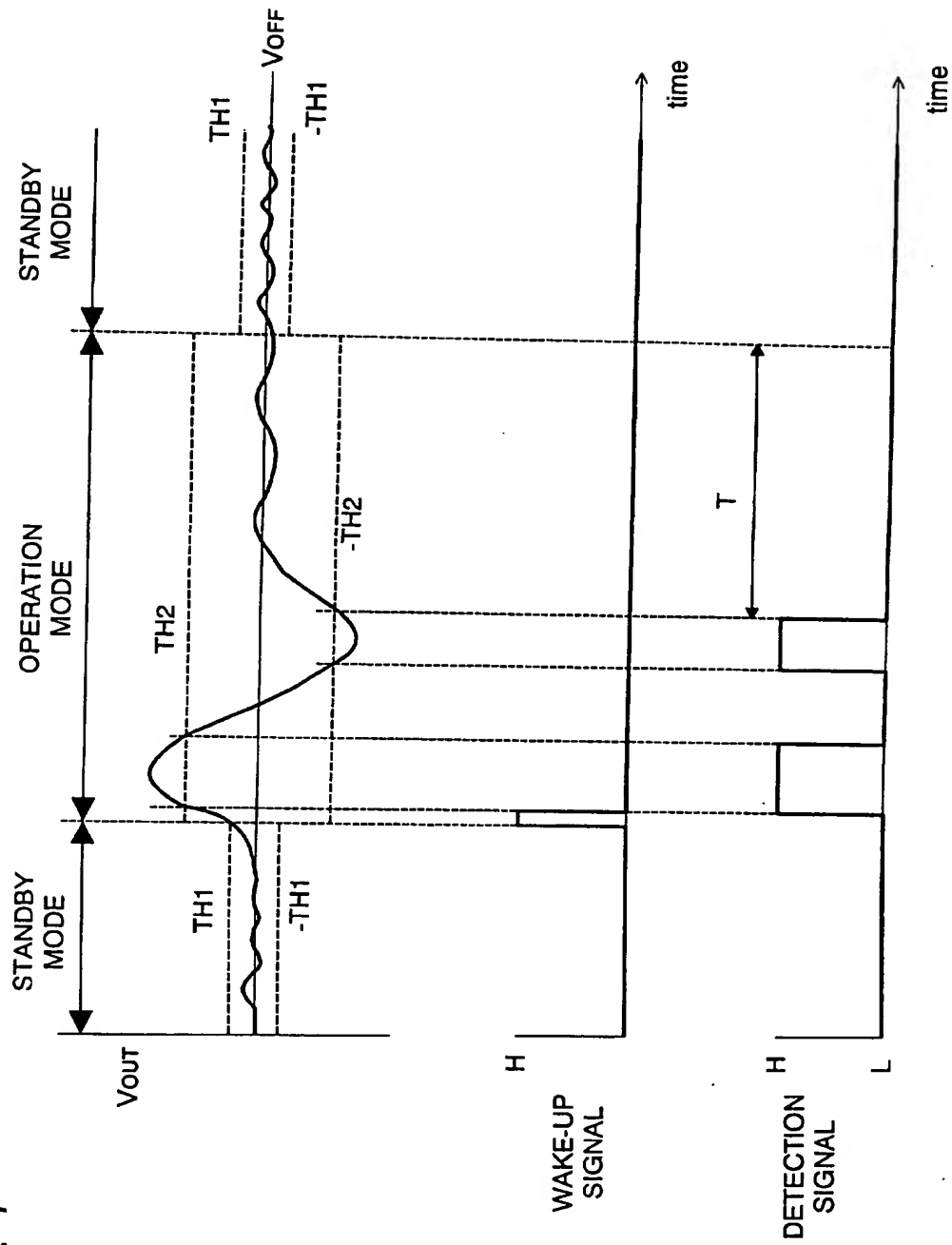


FIG. 6

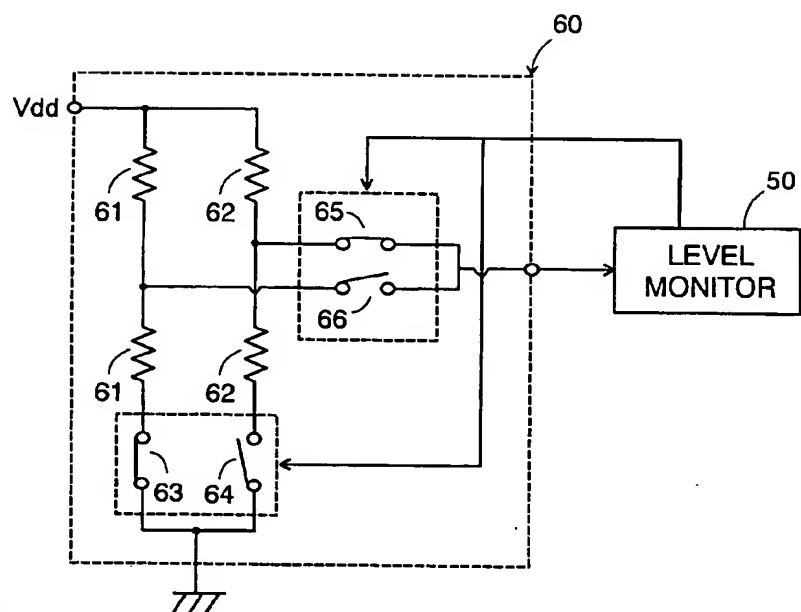


FIG. 8

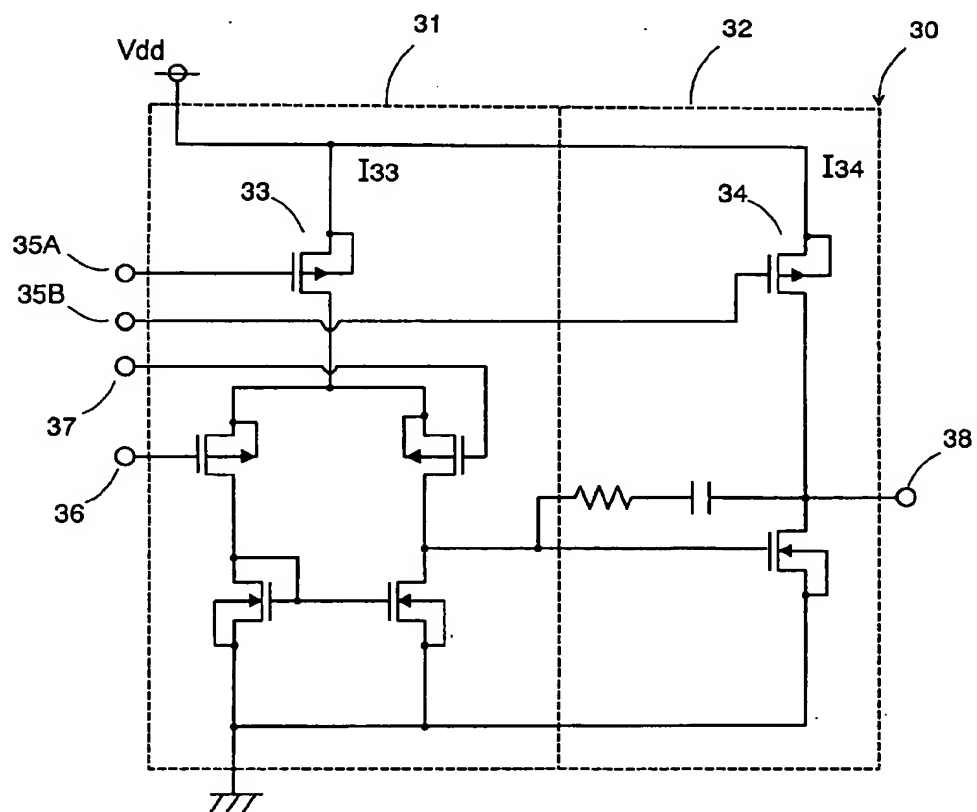


FIG. 7

